XUSB2104&2102 Product Brief

1. Overview

The XUSB2104/2102 are Universal Serial Bus 3.0 host controllers, which comply with Universal Serial Bus 3.0 Specification, and Intel's eXtensible Host Controller Interface(xHCI). These devices reduce power consumption and offer a smaller package footprint making them ideal for designers who wish to add the USB3.0 interface to mobile computing devices such as laptops and notebook computers.

The XUSB2104 supports four USB3.0 SuperSpeed ports and the XUSB2102 supports two USB3.0 SuperSpeed ports. The XUSB2104/2102 use a PCI Express Gen 2 system interface bus allowing system designers to easily add up to four USB3.0 SuperSpeed ports to systems containing the PCI Express bus interface. When connected to USB 3.0 compliant peripherals, XUSB2104/2102 can transfer information at clock speeds of up to 5Gbps. The XUSB2104/2102 USB 3.0 standard are fully compliant and backward compatible with the previous USB2.0 standard. The new USB 3.0 standard supports data transfer speeds of up to ten times faster than those of the previous-generation USB2.0 standard, enabling quick and efficient transfers of large amounts of information.

2. Features

- 1.1V core and 3.3V I/O power supplies.
- Reference clock frequency of 24 MHz, generated by an external crystal.
- PCIe 2.0 endpoint device
- Compliant with PCIe 2.0 specifications
- Supports communication at speed of 2.5 Gbps and 5 Gbps
- Supports aggressive power management
- Supports error reporting, recovery and correction
- Supports Message Signaled Interrupt (MSI&MSI-X)
- Improved PCIe read request efficiency
- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc
- Supports the following speed data rates: Low-Speed (1.5 Mbps) /

XUSB2104&2102 Product Brief

Full-Speed (12 Mbps) / Hi-Speed (480 Mbps) / SuperSpeed (5 Gbps)

- Supports all USB compliant data transfer types as follows; Control / Bulk / Interrupt /Isochronous transfer
- Compliant with Intel's eXtensible Host Controller Interface (xHCI) Specification Revision 1.1
- Supports USB debugging capability on all SuperSpeed ports
- Supports USB legacy function
- A four-pin SPI interface provides read and write access to an external SPI flash device for Firmware
- Supports Firmware Download Interface from system BIOS or system software
- Vendor specific information stored in the external device is read by the controller during the chip power-up

3. Application

- Server
- Storage device
- Router
- PCIe card

4. Function Diagram

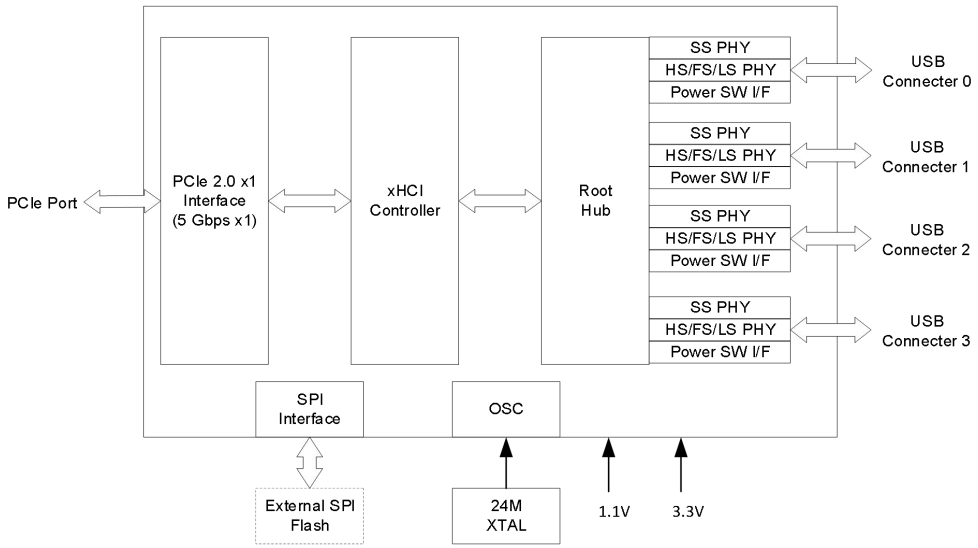

Figure 1 XUSB2104 Architecture

XUSB2104&2102 Product Brief

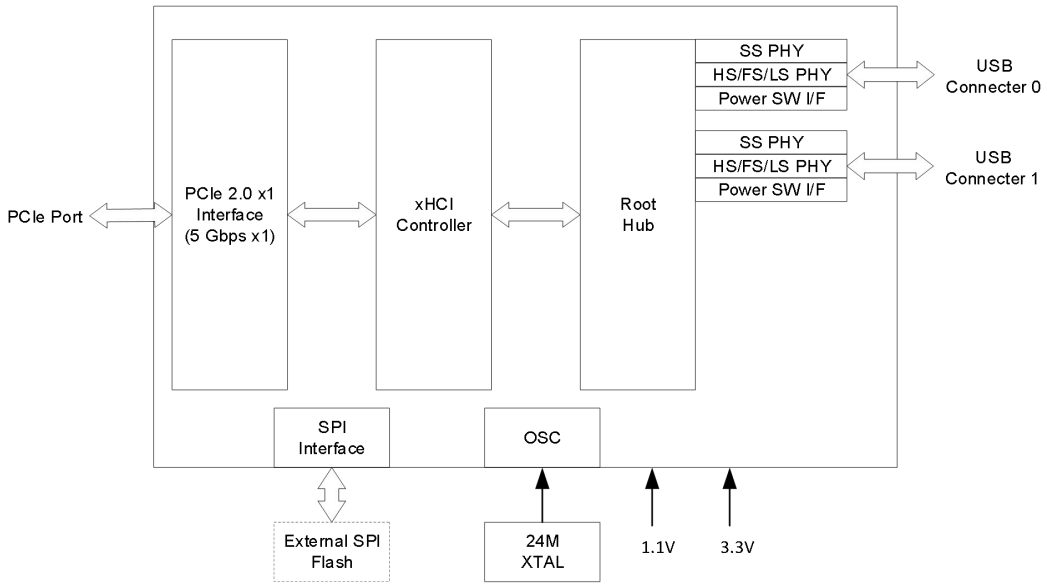

Figure 2. XUSB2102 Architecture

PCIe 2.0 x1 Interface	**Comply with PCI Express Gen2 interface, with 1 lane. This block includes both the link and PHY layers.**
xHCI Controller	Handles all support required for USB 3.0, SuperSpeed and Hi-/Full-/Low-Speed.This block includes the register interface from the system.
Root hub	Hub function in host controller.
SS PHY	For SuperSpeed Tx/Rx
HS/FS/LS PHY	For Hi-/Full-/Low-Speed Tx/Rx
Power SW I/F	Connected to external power switch for port power control and over current detection.
SPI Interface	Connected to external serial Flash. When system BIOS or system software does not support FW download function, the external serial Flash is required.
OSC	Internal oscillator block.